AMENDMENTS TO THE CLAIMS

1. (Original) An automated method for designing integrated circuits (ICs), comprising the steps of:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block; and

generating at least one design-specific cell representative of said functional block, said design-specific cell generated based on said design objective of said IC.

2. (Currently amended) The method of claim 1, wherein said step of generating comprises evaluating said design-specific cell based on ~~the~~ a context of use for ~~in which~~ said design-specific cell ~~is to be used~~.

3. (Currently amended) The method of claim 1, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set ~~of~~ comprising at least one cell, based on said IC design objective.

4. (Currently amended) The method of claim 3, wherein said step of characterizing and selecting is repeated until the design ~~specific~~ objective is met.

5. (Currently amended) The method of claim 1, wherein said design objective is selected from the group consisting of: IC design die size, die ~~(~~area~~)~~, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

6. (Original) The method of claim 1, further comprising a step of optimizing said IC design.

7. (Original) The method of claim 6, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

8. (Original) The method of claim 6, wherein said step of optimizing is performed automatically.

9. (Currently amended) The method of claim 8, wherein said ~~step of~~ optimizing is repeated until said IC design meets at least one optimization metric.

10. (Original) The method of claim 1, wherein said design-specific cell is a transistor-level cell.

11. (Currently amended) A system for implementing an automated integrated circuit (IC) design process, said system comprising:

a ~~means for describing~~ description of said IC, said description including at least one design objective of said IC;

a local optimization control for partitioning said description into at least one functional block; and

a design-specific cell generatio~~r~~n ~~means~~ for generating at least one design-specific cell representation of the functional block, said design-specific cell generated based on said design objective of said IC.

12. (Currently amended) The system of claim 11, further comprising an analysis control module ~~means~~ for evaluating said design-specific cell based ~~i~~on ~~the~~ a context of use for ~~in which~~ said design-specific cell ~~is to be used~~.

13. (Currently amended) The system of claim 11, further comprising ~~means~~ a control module for characterizing and selecting said design-specific cell from a minimal set ~~of~~ comprising at least one cell, based on said IC design objective.

14. (Currently amended) The system of claim 13, wherein said ~~means~~ control module for characterizing and selecting is repeated until said design-~~specific~~ objective is satisfied.

15. (Currently amended) The system of claim 11, wherein said design-specific cell generati~~o~~r~~n means~~ selects said design objective from a group consisting of: IC design die size, die ~~(~~area~~)~~, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability, and cost.

16. (Currently amended) The system of claim 11, further comprising ~~means~~ an optimizer for optimizing said IC design.

17. (Currently amended) The system of claim 16, wherein a criteria used by said ~~means~~ optimizer ~~for optimizing~~ is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

18. (Currently amended) The system of claim 16, wherein said ~~means~~ optimizer ~~for optimizing~~ is ~~performed~~ operated automatically.

19. (Currently amended) The system of claim 16, wherein said ~~means for~~ optimize~~ring~~ is iteratively ~~optimized~~ operated until said IC design meets at least one optimization metric.

20. (Currently amended) The system of claim 11, wherein said design-specific cell generatiorn ~~means is capable of~~ generatesing a transistor-level design-specific cell.

21. (Original) A design-specific cell produced by an automated IC design process, said IC design process comprising:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block; and

generating at least one design-specific cell representative of said ~~the~~ functional block, said design-specific cell generated based on the design objective of said IC.

22. (Currently amended) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises evaluating said design-specific cell based on ~~the~~ a context of use ~~in which~~ for said design-specific cell ~~is to be used~~.

23. (Currently amended) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process characterizes and selects said design-specific cell from a minimal set ~~of~~ comprising at least one design-specific cell, based on said IC design objective.

24. (Currently amended) The design-specific cell produced by said IC design process of claim 23, wherein said IC design process is repeated until said design ~~specific~~ objective is met.

25. (Currently amended) The design-specific cell produced by said IC design process of claim 21, wherein said design objective of said IC design process is selected

from the group consisting of: IC design die size, die ~~(area)~~, performance, power consumption, signal integrity, routability, fault tolerance, testability, reliability, and cost.

26. (Original) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises a step of optimizing said IC design.

27. (Original) The design-specific cell produced by said IC design process of claim 26, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

28. (Original) The design-specific cell produced by said IC design process of claim 21, wherein said step of optimizing is performed automatically.

29. (Original) The design-specific cell produced by said IC design process of claim 28, wherein said step of optimizing is repeated until said IC design satisfies at least one optimization metric.

30. (Original) A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit (IC), said storage medium comprising:

program instructions for describing the IC, the description including at least one design objective of said IC;

program instructions for partitioning said description into at least one functional block; and

program instructions for generating at least one design-specific cell representative of the functional block, said design-specific cell generated based on the design objective of said IC.

31. (New) An automated method for designing integrated circuits (ICs), comprising the steps of:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block;

generating at least one design-specific cell representative of said functional block, said design-specific cell generated based on said design objective of said IC; and

automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one optimization metric.

32. (New) The method of claim 31, wherein said step of generating comprises evaluating said design-specific cell based on a context of use for said design-specific cell.

33. (New) The method of claim 31, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

34. (New) The method of claim 33, wherein said step of characterizing and selecting is repeated until the design objective is met.

35. (New) The method of claim 31, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

36. (New) The method of claim 31, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

37. (New) The method of claim 31, wherein said step of optimizing is repeated until said optimized IC design meets at least one optimization metric.

38. (New) The method of claim 31, wherein said design-specific cell is a transistor-level cell.

39. (New) A system for implementing an automated integrated circuit (IC) design process, said system comprising:

a description of said IC, said description including at least one design objective of said IC;

a local optimization control for partitioning said description into at least one functional block;

a design-specific cell generator for generating at least one design-specific cell representation of the functional block, said design-specific cell generated based on said design objective of said IC; and

an optimizer for automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one optimization metric.

40. (New) The system of claim 39, further comprising an analysis control module for evaluating said design-specific cell based on a context of use for said design-specific cell.

41. (New) The system of claim 39, further comprising a control module for characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

42. (New) The system of claim 41, wherein said control module is repeated until said design objective is satisfied.

43. (New) The system of claim 39, wherein said design-specific cell generator selects said design objective from a group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability, and cost.

44. (New) The system of claim 39, wherein a criteria used by said optimizer is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

45. (New) The system of claim 39, wherein said optimizer iteratively optimizes said IC design until said IC design meets at least one optimization metric.

46. (New) The system of claim 39, wherein said design-specific cell generator generates a transistor-level design-specific cell.

47. (New) A design-specific cell produced by an automated IC design process, said IC design process comprising:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block;

generating at least one design-specific cell representative of said ~~the~~ functional block, said design-specific cell generated based on the design objective of said IC; and

automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one optimization metric.

48. (New) The design-specific cell produced by said IC design process of claim 47, wherein said IC design process further comprises evaluating said design-specific cell based on a context of use for said design-specific cell .

49. (New) The design-specific cell produced by said IC design process of claim 47, wherein said IC design process characterizes and selects said design-specific cell from a minimal set comprising at least one design-specific cell, based on said IC design objective.

50. (New) The design-specific cell produced by said IC design process of claim 49, wherein said IC design process is repeated until said design objective is met.

51. (New) The design-specific cell produced by said IC design process of claim 47, wherein said design objective of said IC design process is selected from the group consisting of: IC design die size, die area, performance, power consumption, signal integrity, routability, fault tolerance, testability, reliability, and cost.

52. (New) The design-specific cell produced by said IC design process of claim 47, wherein a criteria for said optimizing is selected from the group consisting of:

clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

53. (New) The design-specific cell produced by said IC design process of claim 47, wherein said optimizing is repeated until said IC design satisfies at least one optimization metric.

54. (New) A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit (IC), said storage medium comprising:

program instructions for describing the IC, the description including at least one design objective of said IC;

program instructions for partitioning said description into at least one functional block; and

program instructions for generating at least one design-specific cell representative of the functional block, said design-specific cell generated based on the design objective of said IC; and

program instructions for automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one optimization metric.

55. (New) The storage medium of claim 54, wherein said program instructions for generating comprises program instructions for evaluating said design-specific cell based on a context of use for said design-specific cell.

56. (New) The storage medium of claim 54, wherein said program instructions for generating comprises program instructions for characterizing and

selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

57. (New) The storage medium of claim 56, wherein said program instructions for characterizing and selecting is repeated until the design objective is met.

58. (New) The storage medium of claim 54, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

59. (New) The storage medium of claim 54, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

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60. (New) The storage medium of claim 54, wherein said program instructions for optimizing is repeated until said optimized IC design meets at least one optimization metric.

61. (New) The storage medium of claim 54, wherein said design-specific cell is a transistor-level cell.

Claims 1-61 are in the patent application.

The drawings, in particular Figures 1-6, were objected to by the Office. Figures 1-6 have been corrected as indicated in the proposed corrected drawings submitted herewith. Accordingly, it is respectfully requested that the objection to the drawings be reconsidered and withdrawn.

Claims 2-5, 12-15, 21, 22, 24, and 25 were objected to for containing various informalities. Applicants submit that the noted informalities have been fully addressed and corrected as indicated in the amendments thereof submitted herewith.

Claims 9, 19, and 29 were rejected under 35 USC 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. This rejection is respectfully traversed.

Applicants respectfully submit that the subject claims concisely and unambiguously state, as in claim 9 for example, optimizing is repeated until the IC design meets at least one optimization metric. The cooperative relationship between the claimed IC design objectives and the claimed optimization metric should be clear to one of ordinary skill in the art of the invention. Support for Applicants' claim language and reasoning can be found in the specification at least at page 10, ln. 15-18.

Thus, it is not seen as necessary, in view of the cited and relied upon references, the need for claims 9, 19, and 29 to include with greater specificity what optimization metrics are. Accordingly, it is requested that the rejection of claims 9, 19, and 29 be reconsidered and withdrawn.

Applicants acknowledge with appreciation, the Office's indication of allowable subject matter. In particular, it was indicated that claims 9, 19, and 29 would be

allowable if rewritten to overcome the 35 USC 112, second paragraph rejection and include all of the limitations of the base and intervening claims.

Based on the Office's indication of allowable subject matter for claims 9, 19, and 29, independent claims 31, 39, and 47 have been added to the application. Claims 31, 39, and 47 correspond to rewritten versions of claims 9, 19, and 29, respectively. Accordingly, claims 31, 39, and 47 are believed to be in a condition for allowance.

Claims 32-38 depend from claim 31, claims 40-46 depend from claim 39, and claims 48-53 depend from claim 47.

Therefore, it is respectfully submitted that claims 31-53 are in a condition for allowance.

Regarding newly added claim 54, it is respectfully submitted that claim 54 is directed to a storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit, worded similarly to claim 9. Therefore, it is respectfully submitted that claim 54, and claims 55-60 depending from claim 54, are all in a condition for allowance.

Regarding the 35 USC 102 rejection of claims 1, 2, 20, 21, and 30 under 35 USC 102(e) as being anticipated by Gan et al. (hereinafter Gan), the rejection is traversed.

The Office alleges that Gan discloses partitioning the description of the IC design into at least one functional block, citing col. 4, ln. 12-21. It is respectfully submitted that the "partitioning" disclosed in Gan is not the same as the partitioning claimed by Applicants in claims 1, 20, and 30.

It is first noted that Gan is directed to and discloses a methodology for controlling the physical layout design of an IC, given a circuit netlist. The cells disclosed in Gan act as place-holders (see Abstract). That is, not cells with real functionality, whose sole

purpose is to force place-and-route tools to route a selected signal path through a particular physical location on a semiconductor die. The Office's attention is directed to the detailed description of Gan, and in particular to col. 4, ln. 12-21 cited and relied upon by the Office wherein "bounding boxes" are disclosed. As stated in Gan at col. 4, ln. 13-15, "Bounding box" is a term of art that describes the smallest area that encloses all of the geometry of circuit design of cell. (emphasis added) Gan is concerned with the size of the block, not the function (i.e., a functional block) as claimed. For example, Gan further discloses that in one embodiment the high-level physical description is a library exchange format (LEF) data file (Gan, col. 4, ln. 21-22). It is noted that the LEF data file format includes no representative functional data, only rectangle coordinates (i.e., size) data.

Therefore, the Gan disclosed phantom blocks 220 and 230 within bounding boxes 235 and 240 are not the same as Applicants' claimed "partitioning the description into at least one functional block". The Gan bounding boxes (or any other disclosed grouping) are not the same as Applicants' claimed "partitioning into at least one functional block".

Accordingly, Gan fails to anticipate claims 1, 20, and 30 since Gan fails to disclose each and every element, configured as claimed by Applicants. It is respectfully submitted that claims 1, 20, and 30 are patentable over Gan under 35 USC 102(e).

Claims 2 and 21 depend from claims 1 and 20, respectively. Therefore, it is respectfully submitted that claims 2 and 21 are patentable over Gan for at least the reasons stated above regarding claims 1and 20.

Regarding the rejection of claims 1-8, 11-18, and 21-28 under 35 USC 102(e) as being anticipated by Katsioulas et al. (hereinafter Katsioulas), this rejection is traversed.

It is first noted that Katsioulas discloses a way of placing-and-routing large designs made of standard-cells using what is referred to therein as a STANDARD BLOCK architecture (col. 3, ln. 21-36). Katsioulas is a physical design abstraction methodology, similar to Gan. Thus, Katsioulas is not concerned with the functionality

(and optimizing the functionality) at various levels of abstraction (e.g., Boolean logic level, transistor level, etc.) as is Applicants' claimed invention. This point is made clear by Katsioulas where it is disclosed that "[B]y providing the STANDARD BLOCKs as a physical representation at a higher abstraction level than standard cells and by eliminating the irregularity associated with functional blocks, the STANDARD BLOCK architecture enables increased IC layout density, improved timing, and higher reliability." (Katsioulas, col. 4, ln. 38-45)

In fact, Katsioulas appears to teach away from partitioning a description of the IC design into functional blocks.

Referring to the section of Katsioulas cited and relied upon by the Office for partitioning, it is noted that col 10, ln. 65- col. 11, ln. 8 do not disclose partitioning the IC design into functional blocks. Katsioulas discloses only STANDARD BLOCK architecture, as discussed above. While it is disclosed that the "partitioning is based, for example, on functionality, number of gates (or cells), number of pins per STANDARD BLOCK, total dimensions of the chip, etc.", there is no disclosure that the STANDARD BLOCK departs from the STANDARD BLOCK architecture as disclosed and discussed above. That is, there is no disclosure in Katsioulas to partition the IC design into functional blocks rather than the disclosed STANDARD BLOCKs.

Accordingly, Katsioulas fails to anticipate claim 1, 11, and 21 since Katsioulas fails to disclose each and every element, configured as claimed by Applicants. It is respectfully submitted that claims 1, 11, and 21 are patentable over Katsioulas under 35 USC 102(e).

Claims 2-8, 12-18, and 22-29 depend from claims 1, 11, and 21, respectively. Therefore, it is respectfully submitted that claims 2-8, 12-18, and 22-29 are patentable over Katsioulas for at least the reasons stated above regarding claims 1, 11, and 21.

Accordingly, the swift and favorable allowance of claims 1-60 is earnestly solicited.

Respectfully submitted,

Date: 6-27-03

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